IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Application Branch

In re Patent Application of
Applicants : Kazuo SUTO

Serial No. : Not Yet Known

Filed : CONCURRENTLY

For : MODULATOR

Attorney Docket: 32014-177530

PRELIMINARY AMENDMENT

January 24, 2002

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination please amend Claims 4, 6, 9 and 11 as follows:

4. (amended) The modulator as claimed in Claim 2, wherein the PLL circuit includes an oscillator that generates the reference signal, a frequency divider that divides the frequency of the input signal to output a frequency divided signal, and a comparator that compares the reference signal and the frequency divided signal to detect a phase difference between both.

6. (amended) The modulator as claimed in Claim 2, wherein the AGC circuit outputs the control signal on the basis of the signal outputted from the PLL circuit.

9. (amended) The modulator as claimed in Claim 7, wherein the PLL circuit includes an oscillator that generates the reference signal, a frequency divider that divides the frequency of the input signal to output a frequency divided signal, and a comparator that compares the reference signal and the frequency divided signal to detect a phase difference between both.

11. (amended) The modulator as claimed in Claim 7, wherein the AGC circuit outputs the control signal on the basis of the signal outputted from the PLL circuit.

REMARKS

This Preliminary Amendment is being filed in order to eliminate the multiple dependency of the claims. An action on the merits of Claims 1-19 is requested.

Respectfully submitted,

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Marked-Up Copy of Amended Claims:

4. (amended) The modulator as claimed in Claim 2 [or Claim 3], wherein the PLL circuit includes an oscillator that generates the reference signal, a frequency divider that divides the frequency of the input signal to output a frequency divided signal, and a comparator that compares the reference signal and the frequency divided signal to detect a phase difference between both.

6. (amended) The modulator as claimed in Claim 2 [or Claim 3], wherein the AGC circuit outputs the control signal on the basis of the signal outputted from the PLL circuit.

9. (amended) The modulator as claimed in Claim 7 [or Claim 8], wherein the PLL circuit includes an oscillator that generates the reference signal, a frequency divider that divides the frequency of the input signal to output a frequency divided signal, and a comparator that compares the reference signal and the frequency divided signal to detect a phase difference between both.

11. (amended) The modulator as claimed in Claim 7 [or Claim 8], wherein the AGC circuit outputs the control signal on the basis of the signal outputted from the PLL circuit.